IEEE International Conference on

Electrical Performance of Electronic Packages and Systems (EPEPS-2011)

San Jose, Oct. 23-26

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Advance Program

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Sunday, October 23, 2011

Session S-I

1:00 - 2:40 Sunday Tutorial - Part I

Chairs: Kathleen L. Melde, Uni. of Arizona, Tucson
Ram Achar, Carleton University, Canada

Room: Donner/Siskiyou

Half Day Tutorial:

S-Parameters to X-Parameters: From Concept to Practice with Linear & Nonlinear Systems for Signal Integrity Design, Modeling, Simulation & Measurements

Presented By: Mike Resso & David Root, Agilent Technologies, Santa Rosa, CA

2:40 - 3:00 S-II: Coffee Break

Room: Bayshore Foyer

Session S-III

3:00 - 4:30 Sunday Tutorial - Part II

Chairs: Kathleen L. Melde, Uni. of Arizona, Tucson

Room: Donner/Siskiyou

S-Parameters to X-Parameters: Tutorial by Mike Resso & David Root is continued

Session S-IV

4:40 - 5:30 TC-12 Meeting (EDMS)

Chairs: Madhavan Swaminathan, GIT, Atlanta
Dale Becker, IBM, Poughkeepsie

Room: Donner/Siskiyou

Session S-V

5:30 - 7:30 Welcome Reception

Room: Donner/Siskiyou/Club Max

Conference Reception

Session S-VI

7:00 - 10:00 **EPEPS TPC Meeting**

Chairs: Ram Achar, Carleton University, Canada
Brian Young, Texas Instruments, Austin

Room: Monterey/Carmel

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Monday, October 24, 2011

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7:00 - 8:00 M-I: Breakfast

Room: Cascade/Sierra

Session M-II

8:10 - 8:20 Welcome Notes from the Chair
Chairs: Ram Achar, Carleton University, Canada

Room: Donner/Siskiyou

Session M-III

8:20 - 9:00 Keynote Speech - I
Chairs: Ram Achar, Carleton University, Canada
Dale Becker, IBM, Poughkeepsie

Room: Donner/Siskiyou

Chip-Package-System Convergence: Bridging Multiple Disciplines to Solve Low Power, Cost Down, and System Reliability Challenges

Keynote Speaker: Dr. Andrew Yang, President & Co-founder of Apache Design Inc., VP and GM of ANSYS, Inc.

Session M-IV

9:00 - 10:00 Power Integrity in High-Speed Designs
Chairs: Antonio Maffucci, University di Cassino, Italy
Brian Young, Texas Instruments, Austin

Room: Donner/Siskiyou

- M-IV.1. **Plane Bounce in High-speed Single-ended Signaling I/O Interfaces**

  Dan Oh — Rambus Inc., Sunnyvale

- M-IV.2. **Practical Aspects of Modeling Apertures for Signal and Power Integrity Co-simulation**

  Jae Young Choi, Madhavan Swaminathan — Georgia Institute of Technology, Atlanta

- M-IV.3. **Verfication of Novel Technology for Power Integrity on 16-Channel 3Gbps Circuit Boards**

  Sasaoka Norifumi[*], Ochi Takafumi[*], Akiyama Yutaka[+], Kono Kazuo[+], Ueda Chihiro[+], Otsuka Kanji[+] — [*]Nippon Kodoshi Corporation, Japan, [+]Meisei University, Japan

10:00 - 10:25 **M-V: Coffee Break**

Room: Bayshore Foyer

Session M-VI

10:25 - 11:05 **Design Strategies for Processor, Chip/Package Co-Design**
Chairs: Paul Franzon, North Carolina State Uni., Raleigh
Liu En-Xiao, IHPC, Singapore

Room: Donner/Siskiyou

- M-VI.1. **Deriving Voltage Tolerance Specification for Processor Circuit Design**

  Tingdong Zhou, Joshua D. Friedrich, Wiren Becker — IBM, Austin

- M-VI.2. **Early Stage Chip/Package/Board Co-design Tecgniques for System-on-Chip**

  Sode Tanaka Mikiko, Toyama Masahiro, Mori Ryo, Nakashima Hidenari, Haida Masahiro, Ooshima Izumi — Renesas Electronics Corporation, Japan

Session M-VII

11:05 - 12:05 **Novel RF and Chip-to-Chip Interconnects**
Chairs: Hartmut Grabinski, University of Hannover, Germany
Daniel de Araujo, Nimbic Inc., Mountain View

Room: Donner/Siskiyou

- M-VII.1. **High-Density Silicon Carrier Transmission Line Design for Chip-to-Chip Interconnects**

  Xiaoxiong (Kevin) Gu, Lavanya Turlapati, Bing Dang, Cornelia Tsang, Paul Andry, Timothy Dickson, Michael Beakes, John Knickerbocker, Daniel Friedman — IBM T. J. Watson Research Center, New York

- M-VII.2. **Wireless RF Data Communications Using 60 GHz Antennas in Multi-Core Systems**

  Ho-Hsin Yeh, Nobuki Hiramatsu, Kathleen Melde — University of Arizona, Tucson

- M-VII.3. **Electrical Performance of Vertical Natural Capacitor for RF System-on-Chip in 32-nm Technology**

  Liu En-Xiao, Li Er-Ping — Institute of High Performance Computing, Singapore

12:05 - 2:00 **M-VIII: Lunch Break; EPEPS-TPC Meeting**

Room: Cascade-Sierra

Session M-IX

2:00 - 3:20 **Macromodeling and Circuit Analysis**

Chairs: Michel Nakhla, Carleton University, Canada
Ruey-Beei Wu, NTU, Taiwan

Room: Donner/Siskiyou

- M-IX.1. **Alternative SPICE Implementation of Circuit Uncertainties based on Orthogonal Polynomials**

  Paolo Manfredi, Igor Stievano, Flavio Canavero — Politecnico di Torino, Italy

- M-IX.2. **Sequential Sampling Strategy for the Modeling of Parameterized Microwave and RF Components**

  Dirk Deschrijver, Karel Crombecq, Huu Minh Nguyen, Tom Dhaene — Ghent University - IBBT, Belgium

- M-IX.3. **Fast Rational Function Fitting of Broadband Multi-Port Responses Via Repeated Random Sampling**

  Joon Hyung Chung, Andreas C. Cangellaris — University of Illinois at Urbana Champaign

- M-IX.4. **A Compression Strategy for Rational Macromodeling of Large Interconnect Structures**

  Stefano Grivet-Talocia, Salvatore Bernardo Olivadese, Piero Triverio — Politecnico di Torino, Italy

3:20 - 3:50 M-X: Coffee Break

Room: Bayshore Foyer

Session M-XI

3:50 - 4:30 Jitter Modeling and Analysis

Chairs: Wendem Beyene, Rambus Inc., Sunnyvale
Dan Jiao, Purdue University, West Lafayette

Room: Donner/Siskiyou

- M-XI.1. **Spectral Relations of Supply Noise and Jitter with Regular and Feed Forward Clocking Schemes**

  Omer Vikinski — Intel Corporation, Israel

- M-XI.2. **Extraction of Jitter Parameters from BER Measurements**

  Marko Aleksic — Rambus Inc., Sunnyvale

Session M-XII

4:30 - 7:30 Poster Session and Industry Reception

Chairs: Albert Ruehli, Missouri Univ. Science & Technology, Rolla
Dan Oh, Rambus Inc., Sunnyvale

Room: Cascade-Sierra

- M-XII.1. **Modeling of ISI in High Speed Serial I/Os Terminated with Discontinuities**

  Aritra Dey[*], Hong Jiang Song[+] — [*]Arizona State University, Tempe, [+]Intel Corporation, Chandler

- M-XII.2. **SI-Aware Layout and Equalizer Design to Enhance Performance of High-Speed Links in Blade Servers**

  Yung-Shou Cheng[*], Hsin-Hung Lu[*], Michael Chang[+], Stephen Chang[+], Bob Liu[+], Ruey-Beei Wu[*] — [*]National Taiwan University, Taiwan, [+]Portwell Technology Inc., Taiwan

- M-XII.3. **Switching Regulator Noise Coupled onto High Speed Differential Links**

  Daniel Rodriguez, Sungjun Chun, Rohan Mandrekar, Daniel Dreps — IBM, Austin

- M-XII.4. **3D Via Modeling Simplification on Multilayer Mid-planes**

  Qian Li[*], Kathleen L. Melde[*], Gong-Jong Yeh[+], Hui Wu[+], Yaochao Yang[+] — [*]University of Arizona, Tucson, [+]Cisco Systems, San Jose

- M-XII.5. **Common-Mode Noise Reduction Schemes for Differential Serpentine Delay Microstrip Line in High-Speed Digital Circuits**

  Guang-Hwa Shiue, Yi-Chin Tsai , Che-Ming Hsu, Jia-Hung Shiu — Chung Yuan Christian University, Taiwan

- M-XII.6. **Design of a 12Gb/s Transceiver for High-Density Links with Discontinuities using Modal Signaling**

  Pavle Milosevic, Jose Schutt-Aine — University of Illinois at Urbana-Champaign

- M-XII.7. **A De-embedding Method for Extracting S-Parameters of Vertical Interconnect in Advanced Packaging**

  Yin-Cheng Chang[*], Shawn S. H. Hsu[*], Da-Chiang Chang[*], Jeng-Hung Lee[+], Shuw-Guann Lin[+], Ying-Zong Juang[+] — [*]National Tsing Hua University, Taiwan, [+]National Applied Research Laboratories, Taiwan

- M-XII.8. **Passive Model-Order Reduction of RLC Circuits with Embedded Time-Delay Descriptor Systems**

  Andrew Charest, Michel Nakhla, Ram Achar — Carleton University, Canada

- M-XII.9. **A New Method to Estimate Phases of Sinusoidal Jitter to Evaluate High-Speed Links**

  Yu Chang, Chris Madden, Ralf Schmitt — Rambus Inc., Sunnyvale

- M-XII.10. **Electrical Performances of Inkjet Printed Flexible Cable ECG Monitoring**

  Qiansu Wan, Geng Yang, Qiang Chen, Lirong Zheng — Royal Institute of Technology (KTH), Sweden

- M-XII.11. **Decoupling Capacitor Stacked Chip (DCSC) in TSV-based 3D-ICs**

  Eunseok Song, Kyoungchoul koo, Myunghoi Kim, Jun So Pak, Joungho Kim — KAIST, Korea

- M-XII.12. **A Fine-Grained Co-Simulation Methodology for IR-drop Noise in Silicon Interposer and TSV-based 3D IC**

  Taigon Song, Sung Kyu Lim — Georgia Institute of Technology, Atlanta

- M-XII.13. **High-Frequency Through-Silicon Via (TSV) Failure Analysis**

  Joohee Kim[*], Jonghyun Cho[*], Jun So Pak[*], Joungho Kim[*], Jong-Min Yook[+], Jun Chul Kim[+] — [*]KAIST, Korea, [+]KETI, Korea

- M-XII.14. **Temperature-Dependent Thorough-Silicon Via (TSV) Model and Noise Coupling**

  Manho Lee[*], Jonghyun Cho[*], Joohee Kim[*], Jun So Pak[*], Joungho Kim[*], Hyungdong Lee[+], Junho Lee[+], Kunwoo Park[+] — [*]KAIST, Korea, [+]Hynix Semiconductor Inc., Korea

- M-XII.15. **Signal-Integrity improvement based on the Segmental-Transmission-Line**

  Hiroki Shimada[*], Shohei Akita[*], Masami Ishiguro[*], Moritoshi Yasunaga[*], Ikuo Yoshihara[+] — [*]University of Tsukuba, Japan, [+]University of Miyazaki, Japan

- M-XII.16. **Waveform Relaxation based Analysis of Noise Propagation in Power Distribution Networks**

  Sourajeet Roy, Anestis Dounavis — University of Western Ontario, Canada

- M-XII.17. **Reduced Circuit Modeling of Mother Board and Package for a System Power Delivery Analysis**

  Jayong Koo, Vishram Pandit — Intel Corporation, Folsom

- M-XII.18. **Application of the Latency Insertion Method to Electro-Thermal Circuit Analysis**

  Dmitri Klokotov[*], Jose Schutt-Aine[*], Wendem Beyene[+], Don Mullen[+], Ming Li[+], Ralf Schmitt[+], Ling Yang[+] — [*]University of Illinois at Urbana-Champaign, [+]Rambus Inc., Sunnyvale

- M-XII.19. **Analysis and Approach of TSV-Based Hierarchical Power Distribution Networks for Estimating 1st Droop and Resonant Noise in 3DIC**

  Gary Charles[*], Paul Franzon[*], Jaemin Kim[+], Alex Levin[**] — [*]North Carolina State University, Raleigh, [+]IMEC, Belgium, [**]Intel

Corporation, Washington

- M-XII.20. **Capacitance Calculation for a Shared-Antipad Via Structure Using an Integral Equation Method Based on Partial Capacitance**

  Hanfeng Wang, Albert Ruehli, Jun Fan — Missouri University of Science and Technology, Rolla

- M-XII.21. **Three Finite-Element Time-Domain–Based Numerical Algorithms for High-Frequency Broadband PCB Simulations**

  Xiaolei Li[*], Jian-Ming Jin[*], Jilin Tan[+] — [*]University of Illinois at Urbana-Champaign, [+]Cadence Design Systems, Chelmsford

- M-XII.22. **CAD Model Reconstruction of Solder Balls for the Computationally Efficient Electromagnetic Field Simulation**

  Juergen Hillebrand, Steffen Kiess, Yu Wang, Marek Wroblewski, Sven Simon — University of Stuttgart, Germany

- M-XII.23. **Optimal Decoupling Capacitors Design for Suppressing Edge Radiation of Power/Ground Planes**

  Kuan-Wei Li, Kai-Bin Wu, Ruey-Beei Wu — National Taiwan University, Taiwan

- M-XII.24. **Design of Power Delivery Networks using Power Transmission Lines and Pseudo-Balanced Signaling for Multiple I/Os**

  Suzanne Huh, Madhavan Swaminathan, David Keezer — Georgia Institute of Technology, Atlanta

- M-XII.25. **Bended Differential Transmission Line Using Short-Circuited Coupled Line for Common-Mode Noise Suppression**

  Chia-Han Chang, Ruei-Ying Fang, Chun-Long Wang — National Taiwan University of Science and Technology, Taiwan

- M-XII.26. **A Comparison of Two Latency Insertion Methods in Dependent Sources Applications**

  Ping Liu[*], Jilin Tan[+], Zhongyong Zhou[*], Jose Schutt-Aine[**], Patrick Goh[**] — [*]Cadence Design Systems, Shanghai, [+]Cadence Design Systems, Chelmsford, [**]University of Illinois at Urbana-Champaign

- M-XII.27. **Twelve Pseudo-Differential Transmission Schemes**

  Frederic Broyde, Evelyne Clavelier — Excem, France

- M-XII.28. **Compact Stepped-Impedance Resonator Transformer**

  Ruei-Ying Fang, Chia-Fen Liu, Chun-Long Wang — National Taiwan University of Science and Technology, Taiwan

- M-XII.29. **Efficient Spectral Domain Analysis of Multilayered Shielded Microstrip using Two Super Convergent Series**

  Sidharath Jain[*], Jiming Song[*], Telesphor Kamgaing[+], Yidnekachew Mekonnen[+] — [*]Iowa State University, Ames, [+]Intel Corporation, Chandler

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Tuesday, October 25, 2011

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7:00 - 8:00 T-I: Breakfast

Room: Cascade/Sierra

Session T-II

8:00 - 9:20 Measurements Methodologies for Signal Integrity

Chairs: Kathleen L. Melde , Uni. of Arizona, Tucson
Uwe Arz, Physikalisch-Technische Bundesanstalt, Germany

Room: Donner/Siskiyou

- T-II.1. **A Methodology for RF Modeling of Packages using IC Known-Loads**

  Mauro Ballicchia, Marco Farina, Antonio Morini, Tullio Rozzi, Claudio Turchetti, Simone Orcioni — Universita Politecnica delle Marche, Italy

- T-II.2. **Electrical Performance of High Speed Signaling in Coupled Microstrip Lines**

  Darryl Kostka[*], Antonio Ciccomancini Scogna[*], Frank Paglia[+], Bhyrav Mutnury[+] — [*]CST of America, Framingham, [+]Dell Inc., Round Rock

- T-II.3. **Optimized Coplanar Waveguides in Membrane Technology for Wideband On-Wafer Calibrations**

  Uwe Arz, Martina Rohland, Karsten Kuhlmann, Stephanus Buettgenbach — Physikalisch-Technische Bundesanstalt, Germany

- T-II.4. **New Interconnect Evaluation Metrics for High-Speed IO**

  Se-Jung Moon[*], Erkan Acar[*], Richard Mellitz[+] — [*]Intel Corporation, Hillsboro, [+]Intel Corporation, Columbia

Session T-III

9:20 - 10:00 Keynote Speech II

Chairs: Madhavan Swaminathan, GIT, Atlanta
Ram Achar, Carleton University, Canada

Room: Donner/Siskiyou

3D Integration: New Opportunities for Advanced Packaging

Keynote Speaker: Dr. Robert Patti, Chief Technology Officer, Tezzaron Semiconductor Corp.

10:00 - 10:30 **T-IV: Coffee Break**

Room: Bayshore Foyer

Session T-V

10:30 - 11:30 **Emerging Technologies: 3D ICs & Clock Distribution**

Chairs: Xiaoxiong (Kevin) Gu, IBM, NY
Elyse Rosenbaum, UIUC, Urbana Champaign

Room: Donner/Siskiyou

- T-V.1. **Distributed Multi TSV 3D Clock Distribution Network in TSV-based 3D IC**

  Dayoung Kim[*], Joohee Kim[*], Jonghyun Cho[*], Jun So Pak[*], Joungho Kim[*], Hyungdong Lee[+], Junho Lee[+], Kunwoo Park[+] — [*]KAIST, Korea, [+]Hynix Semiconductor Inc., Korea

- T-V.2. **Adaptive Clock Distribution for 3D Integrated Circuits**

  Xi Chen, W Rhett Davis, Paul Franzon — North Carolina State University, Raleigh

- T-V.3. **High-Speed Performance of Silicon Bridge Die-to-Die Interconnects**

  Henning Braunisch, Aleksandar Aleksov, Stefanie Lotz, Johanna Swan — Intel Corporation, Chandler

Session T-VI

11:30 - 12:10 **TSV Modeling**

Chairs: Zhen Mu, Mentor Garphics Corporation, San Jose
Sheldon Tan, University of California, Riverside

Room: Donner/Siskiyou

- T-VI.1. **Through-Silicon Via (TSV) Depletion Effect**

  Jonghyun Cho[*], Myunghoi Kim[*], Joohee Kim[*], Jun So Pak[*], Joungho Kim[*], Hyungdong Lee[+], Junho Lee[+], Kunwoo Park[+] — [*]KAIST, Korea, [+]Hynix Semiconductor Inc., Korea

- T-VI.2. **Impact of Through-Silicon-Via Capacitance on High Frequency Supply Noise in 3D-Stacks**

Amit Trivedi, Wen Yueh, Saibal Mukhopadhyay — Georgia Institute of Technology, Atlanta

12:10 - 1:50 **T-VII: Lunch Break and Luncheon Talk**

Room: Cascade-Sierra

Luncheon Talk Presented by:

Rich Rice, Senior VP, Engineering & Sales, ASE

Session T-VIII

1:50 - 2:50 **Modeling and Simulation of MTLs**

Chairs: Flavio Canavero, Politecnico di Torino, Italy
Zhiping Yang, CISCO Systems Inc., San Jose

Room: Donner/Siskiyou

- T-VIII.1. **Waveform Relaxation and Overlapping Partitioning Techniques for Tightly Coupled Interconnects**

  Mina Farhan[*], Natalie Nakhla[*], Michel Nakhla[*], Ram Achar[*], Albert Ruehli[+] — [*]Carleton University, Canada, [+]University of Missouri Science and Technology, Rolla

- T-VIII.2. **Fast Iterative Simulation of High-Speed Channels via Frequency-Dependent Over-Relaxation**

  Haisheng Hu, Alessandro Chinea, Stefano Grivet-Talocia, Mario Miscuglio — Politecnico di Torino, Italy

- T-VIII.3. **An Analytical Resistive Loss Model for Multiconductor Transmission Lines and the Proof of its Passivity**

  Frederic Broyde, Evelyne Clavelier — Excem, France

Session T-IX

2:50 - 3:30 **Advanced Simulation Methodologies for SI Analysis**

Chairs: Mike Lamson, Texas Instruments (Retd)
Michael Tsuk, ANSYS Inc., Arlington

Room: Donner/Siskiyou

- T-IX.1. **Latency Insertion Method (LIM) for CMOS Circuit Simulations with Multi-rate Considerations**

  Patrick Goh, Jose Schutt-Aine — University of Illinois at Urbana-Champaign

- T-IX.2. **Simulations of Pulse Signals with X-Parameters**

  Nick Huang, Lijun Jiang — The University of Hong Kong

3:30 - 3:55 T-X: Coffee Break

Room: Bayshore Foyer

Session T-XI

3:55 - 5:15 High-Speed Links Design

Chairs: Andreas Weisshaar, Oregon State University, Corvallis
Steve Pytel, Ansys Inc., Pittsburgh

Room: Donner/Siskiyou

- T-XI.1. **Design and Analysis of 12.8 Gb/s Single-Ended Signaling for Memory Interface**

  W. T. Beyene, A. Amirkhany, C. Madden, H. Lan, L. Yang, K. Kaviani, S. Mukherjee, D. Secker, R. Schmitt — Rambus Inc., Sunnyvale

- T-XI.2. **Embedded Equalization for ADC-Based Serial I/O Receivers**

  Keytaek Lee, Ehsan Zhian Tabasy, Samuel Palermo, Ayman Shafik — Texas A&M University, College Station

- T-XI.3. **System Design Considerations for a 5Gb/s Source-Synchronous Link with Common-mode Clocking**

  Jihong Ren[*], Dan Oh[*], Ravi Kollipara[*], Brian Tsang[*], Yue Lu[*], Jared Zerbe[*], Qi Lin[+] — [*]Rambus Inc., Sunnyvale, [+]Nvidia Inc., Santa Clara

- T-XI.4. **Interconnect Channel Characteristics Favoring Double-Edge Pulsewidth Modulation**

  Wei Wang, James Buckwalter — University of California at San Diego

Session T-XII

5:15 - 6:30 Panel Discussion

Room: Donner/Siskiyou

Key Challenges and Future Directions for Design & Analysis of High-Speed Electronic Packages and Interconnects

Moderator: Prof. Vikram Jandhyala, University of Washington, Seattle

Panelists:
Dr. Dian Yang, Apache Design Solutions Inc., San Jose
Dr. George A. Katopis, IBM (Emeritus)
Dr. Andreas Cangellaris, UIUC, Urbana-Champaign
Dr. Madhavan Swaminathan, Georgia Tech, Atlanta
Dr. Devan Iyer, Texas Instruments, Dallas
Judy Priest, Cisco Systems Inc., San Jose
Ken Willis, Sigrity Inc., San Jose

Session T-XIII

6:45 - 10:00 Banquet, Awards Presentation, EPEPS @ 20

Room: Cascade-Sierra

EPEPS@20 : A walk down in the memory lanes

Chairs: Alina Deutsch, IBM (rtd) &
Andreas Cangellaris, UIUC, Urbana-Champaign

Presentations by:

G. (Ari) Arjavalingam - The IEEE Topical Meeting on EPEP: Reflections about its Genesis

Andreas Cangellaris - From EPEE to EPEPS and Beyond

Alina Deutsch - Reflections on 20 Years of the EPEP

George Katopis - The Genesis & Founding Principles of EPEP

Tawfik Rahal-Arabi - EPEPS after Twenty Years

Moises Cases - Nurturing Applied Innovation in a

Fertile Environment - A Rich Mix of Technical and Social Opportunities

Madhavan Swaminathan - EPEP: A Model Conference for the Birth of TC-12(EDMS), SPI, FDIP and EDAPS

Ravi Kaw - Some Anecdotes About EPEP

Ram Achar - EPEPS: transition, current and future

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Wednesday, October 26, 2011

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Session W-I

7:00 - 8:00 Breakfast

Room: Cascade/Sierra

Session W-II

8:10 - 8:50 Embedded Tutorial

Chairs: Jose Schutt-Aine, UIUC, Urbana Champaign
Hideki Asai, Shizuoka University, Japan

Room: Donner/Siskiyou

Fundamentals and Advances in Full-Wave Characterization of Interconnects for PCB Signal Integrity Applications

Presented By: Jianming Jin, UIUC, Urbana-Champaign and
Dennis Nagle and Jilin Tan, Cadence Design Systems Inc., Chelmsford

Session W-III

8:50 - 9:50 EM Methods for Variability Analysis

Chairs: Joungho Kim, KAIST, Korea
Tzong-Lin Wu, NTU, Taiwan

Room: Donner/Siskiyou

- W-III.1. **Macromodeling Based Variability Analysis of an Inverted Embedded Microstrip Line**

  Dries Vande Ginste[*], Daniel De Zutter[*], Dirk Deschrijver[*], Tom Dhaene[*], Flavio Canavero[+]

  [*]Ghent University, Belgium,
  [+]Politecnico di Torino, Italy

- W-III.2. **Interconnect Transient Simulation in the Presence of Layout and Routing Uncertainty**

  Aosheng Rong, Andreas Cangellaris

  University of Illinois at Urbana-Champaign

- W-III.3. **Random Rough Surface Effects in Interconnects Studied by Small Perturbation Theory in Waveguide Model**

  Ruihua Ding[*], Leung Tsang[+], Henning Braunisch[**]

  [*]Intel Corporation, Santa Clara,
  [+]University of Washington, Seattle,
  [**]Intel Corporation, Chandler

9:50 - 10:20 **W-IV: Coffee Break**

Room: Bayshore Foyer

Session W-V

10:20 - 11:00 **Parallel EM Computing for Packages**
Chairs: Stefano Grivet Talocia, Politecnico Di Torino, Italy
Jianming Jin, UIUC, Urbana Champaign

Room: Donner/Siskiyou

- W-V.1. **Towards System-Level Electromagnetic Field Simulation on Computing Clouds**

  Vikram Jandhyala, Dipanjan Gope, Xiren Wang, Don Macmillen, Raul Camposano, Devan Williams, James Pingenot — Nimbic Inc., Mountain View

- W-V.2. **Fast Full-Wave Modeling of Passive Structures with Graphic Processors**

  Andrea G. Chiariello[*], Antonio Maffucci[*], Massimo Nicolazzo[+], Fabio Villone[*] — [*]University of Cassino, Italy, [+]CREATE Consortium, Italy

Session W-VI

11:00 - 12:20 **Advances in EM Algorithms**
Chairs: Henning Braunisch, Intel
Snehamay Sinha, Texas Instruments, Dallas

Room: Donner/Siskiyou

- W-VI.1. **Mixed Integral-Differntial Skin-Effect Models for PEEC Electromagnetic Solver**

  Giulio Antonini[*], Albert Ruehli[+], Lijun Jiang[**] — [*]University of LAquila, Italy, [+]Missouri University of Science and Technology, Rolla, [**]The University of Hong Kong

- W-VI.2. **Full-Wave PEEC Time Domain Solver Based on Leapfrog Scheme**

  Sekine Tadatoshi, Asai Hideki — Shizuoka University, Japan

- W-VI.3. **An Explicit and Unconditionally Stable Time-Domain Finite-Element Method of Linear Compelxity for Electromagnetics-Based Simulation of 3-D Global Interconnect Nework**

  Qing He, Duo Chen, Dan Jiao — Purdue University, West Lafayette

- W-VI.4. **Accuracy-Improved Through-Silicon-Via Model Using Conformal Mapping Technique**

  Tai-Yu Cheng, Chuen-De Wang, Yih-Peng Chiou, Tzong-Lin Wu — National Taiwan University, Taiwan

Session W-VII

12:20 - 2:00 **Lunch Break**

Room: Cascade-Sierra